Claims

1. A method of determining overlay error in an integrated circuit made by a lithographic process comprising:

creating a first layer of the integrated circuit having at least one circuit area including a first active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features, the first layer kerf area including a first measurement feature corresponding substantially to the first layer active circuit feature and separated from the first layer active circuit feature by a distance;

creating a second layer of the integrated circuit having at least one circuit area including a second active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features, the circuit and kerf areas of the first and second layers being substantially superimposed, the second layer kerf area including a second measurement feature corresponding substantially to the second layer active circuit feature and separated therefrom by a distance, the distance of separation between the separated second layer active circuit feature and the second layer kerf measurement feature in the direction that the overlay error is to be determined being the same as the distance of separation between the separated first layer active circuit feature and the first layer kerf measurement feature in such direction, the second layer kerf measurement feature being displaced from the first layer kerf measurement feature compared to the first and second active circuit features in a direction perpendicular to the direction that the overlay error is to be determined;

determining a common point of reference of each of the first and second layer kerf measurement features; and

measuring distance of separation in the direction of overlay error between the common points of reference of each of the first and second layer kerf

measurement features to determine overlay error of the first and second active circuit features.

2. The method of claim 1 wherein the first and second active circuit features corresponding to the first and second layer kerf measurement features contact each other.

3. The method of claim 1 wherein the first and second layers of the integrated circuit each have a plurality of circuit areas separated by kerf areas.

4. The method of claim 1 wherein the second layer kerf measurement feature is displaced from the first layer kerf measurement feature by a distance sufficient to distinguish the corresponding active features in the circuit area so that the first and second layer kerf measurement features are more easily discerned.

5. The method of claim 1 further including cutting apart the plurality of circuit areas and destroying measurement features in the kerf areas.

6. The method of claim 1 wherein the common points of reference of the first and second layer kerf measurement features comprise centerlines of the features.

7. The method of claim 1 wherein the common points of reference of the first and second layer kerf measurement features comprise edges of the features.

8. A method of determining overlay error in a desired direction in an integrated circuit made by a lithographic process comprising:

creating a first layer of the integrated circuit having at least one circuit area including a first active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features, the first layer kerf area

including a first measurement feature corresponding substantially to the first layer active circuit feature and separated from the first layer active circuit feature by a distance;

creating a second layer of the integrated circuit having at least one circuit area including a second active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features, the circuit and kerf areas of the first and second layers being substantially superimposed and the second active circuit feature contacting the first active circuit feature, the second layer kerf area including a second measurement feature corresponding substantially to the second layer active circuit feature and separated therefrom by a distance, the distance of separation between the separated second layer active circuit feature and the second layer kerf measurement feature in the direction that the overlay error is to be determined being the same as the distance of separation between the separated first layer active circuit feature and the first layer kerf measurement feature in such direction, the second layer kerf measurement feature being displaced from the first layer kerf measurement feature compared to the first and second active circuit features in a direction perpendicular to the direction that the overlay error is to be determined;

determining a common point of reference of each of the first and second layer kerf measurement features; and

measuring distance of separation in the direction of overlay error between the common points of reference of each of the first and second layer kerf measurement features to determine overlay error of the first and second active circuit features.

9. The method of claim 8 wherein the first and second layers of the integrated circuit each have a plurality of circuit areas separated by kerf areas.

10. The method of claim 8 wherein the second layer kerf measurement feature is displaced from the first layer kerf measurement feature by a distance sufficient to distinguish the corresponding active features in the circuit area so that the first and second layer kerf measurement features are more easily discerned.

11. The method of claim 8 further including cutting apart the plurality of circuit areas and destroying measurement features in the kerf areas.

12. The method of claim 8 wherein the common points of reference of the first and second layer kerf measurement features comprise centerlines of the features.

13. The method of claim 8 wherein the common points of reference of the first and second layer kerf measurement features comprise edges of the features.

14. An integrated circuit wafer adapted to measure overlay error between layers made by a lithographic process comprising:

a first layer of the integrated circuit having at least one circuit area including a first active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features, the first layer kerf area including a first measurement feature corresponding substantially to the first layer active circuit feature and separated from the first layer active circuit feature by a distance;

a second layer of the integrated circuit having at least one circuit area including a second active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features, the circuit and kerf areas of the first and second layers being substantially superimposed, the second layer kerf area including a second measurement feature corresponding substantially to the second layer active circuit feature and separated therefrom by a distance, the distance of separation between the separated second layer active circuit feature

and the second layer kerf measurement feature in the direction that the overlay error is to be determined being the same as the distance of separation between the separated first layer active circuit feature and the first layer kerf measurement feature in such direction, the second layer kerf measurement feature being displaced from the first layer kerf measurement feature compared to the first and second active circuit features in a direction perpendicular to the direction that the overlay error is to be determined;

common points of reference of each of the first and second layer kerf measurement features being determinable to permit measurement of any separation between the common points of reference of each of the first and second layer kerf measurement features to determine overlay error.

15. The wafer of claim 14 wherein the first and second active circuit features corresponding to the first and second layer kerf measurement features are in contact with each other.

16. The wafer of claim 14 wherein the first and second layers of the integrated circuit each have a plurality of circuit areas separated by kerf areas.

17. The wafer of claim 14 wherein the second layer kerf measurement feature is displaced from the first layer kerf measurement feature by a distance sufficient to distinguish the corresponding active features in the circuit area so that the first and second layer kerf measurement features are more easily discerned.

18. The wafer of claim 14 wherein the measurement features in the kerf areas are adapted to be destroyed when the plurality of circuit areas are cut apart.

19. The wafer of claim 14 wherein the common points of reference of the first and second layer kerf measurement features comprise centerlines of the features.

20. The wafer of claim 14 wherein the common points of reference of the first and second layer kerf measurement features comprise edges of the features.